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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/429,094	10/28/1999	JOHN S. YATES JR.	5231.16	5512

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EXAMINER	
ENG, DAVID Y	

ART UNIT	PAPER NUMBER
2155	21

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/429,094	YATES ET AL.	
	Examiner	Art Unit	
	DAVID Y. ENG	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *04 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52 and 54-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52 and 54-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Applicants are requested to update the status of related applications on page 1 of the specification.

There is no claim 53 in the specification.

Claims 1-52 and 54-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to all independent claims, the recitation "each entry describing a likelihood of the existence of an alternate coding of instructions" is vague and indefinite. It is not clear whether there is or there is no alternate coding of instructions in the system for causing the pipeline to behave differently. Note that the definition of "likelihood" is "probability" in Webster's New Collegiate Dictionary. The probability of existence (instead of "true" or "false") would not result in two outcomes for designating two different behaviors. Note further that a pipeline which is a digital circuit is able to respond to only precise instructions and not probability.

The scope of meaning of the following is not clear:

1. "the architectural definition of the instructions", "an architecturally-visible data manipulation behavior" and "control transfer behavior" in all the independent claims. The Examiner is unable to find their definitions in the specification.

2. "wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt" of claims 19 and 30. The Examiner is unable to find the explanation of the wherein clause in the specification.

3. "altering a manipulation of data or transfer of control behavior of the instruction in a manner incompatible with the architectural definition in an emulated architecture of the instruction" of claim 39. The Examiner is unable to find the support or explanation of the clause.

4. "the architectural definition of the instruction with which the alteration is incompatible is a definition in an emulated architecture" in claims 36-38.

5. "logically equivalent" in claims 22 and 33.

Further with respect to claim 10, it is not clear what actually the instruction pipeline circuitry does.

Claim 14 fails to recite function of the lookup structure. Claim 14 further fails to recite functional relationship between the circuits and the lookup structure such that meaningful operation can be achieved.

Applicants are requested to identify the first table and the second table of claim 57 in the drawings and the description in the specification.

Other dependent claims have similar defects set forth above.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to

make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-52 and 54-57 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification fails to disclose a table lookup circuitry having entries describing a likelihood of the existence of an alternate coding of instructions.

The specification fails to disclose an interrupt circuitry which triggers an interrupt in accordance with interrupt criteria on execution of an instruction , wherein the architectural definition of the instruction does not call for an interrupt, the interrupt criteria being based at least in part on the likelihood of the existence of an alternate coding of instructions (probability) as claimed.

The specification fails to disclose a handler being responsive to the likelihood of the existence of an alternate coding of instructions to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction as claimed.

The specification fails to disclose an instruction pipeline circuitry being affected by the handler being responsive to the likelihood of the existence of an alternate coding of instructions to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction as claimed.

The specification fails to disclose an instruction pipeline circuitry being responsive to the likelihood of the existence of an alternate coding of instructions to alter a manipulation behavior or control transfer behavior of the instruction in a manner incompatible with the architectural definition of the instruction as claimed in claims 10 and 39 for example.

The specification fails to disclose the control of architecturally-visible data manipulation behavior includes changing an instruction set architecture under which instructions are interpreted by the computer of claim 5.

The specification fails to disclose an interrupt circuitry to trigger an interrupt in accordance with **synchronous** interrupt criteria being based on a **memory state** and wherein the architectural definition of the instruction in **an emulated architecture** does not call for an interrupt. The specification further fails to explain what synchronous interrupt criteria, memory state are and what the wherein clause actually means.

Applicants are requested to identify each of the above in the drawings and to identify the disclosure or explanation of the above word-by-word in the specification. Applicants are further requested to identify the disclosure, explanation and support of the invention claimed in each of the 57 claims word-by-word in the specification.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richter (5,481,684).

See at least Figures 1-5 and the description thereof in the specification of Richter.

With respect to independent claims 1, 2, 10, 14, 24, 25, 39, 50 and dependent claims 3-7, 35, 13, 36-38, 15-17, 20, 21, 22, 23, 26, 57, 31-35, 40-47, 49, 51, Richter teaches a microprocessor chip, comprising: an instruction pipeline circuitry (Figure 5, 62 and 48) to effect control transfer from one instrcution set (CISC or RISC) to another (col. 10, line 35-45; col. 9, line 28; col. 5, lines 54 et seq.; col. 3, line 44 and col 2, line 30 et seq.), a table and a lookup circuitry (col 9, line 59 and segment register 10, mode control 42 and mode register) for indicating whether RISC or CISC code is to be decoded (set type bit 21, col 10 line 35), and interrupt circuitry and handler (see interrupts in line 40 column 3 to column 4 line 65).

With respect to calims 8, 14, 24, 25, 30, 27, 28, 48, 52, virtual address and address translation is taught by Richter in line 53 of column 6 and line 52 of column 11.

With respect to calims 11, for the teaching of binary translator, see the two types of decoders in lines 41 of column 12 to the end of column 14.

With respect to calims 19, 30, 9, 12, 18, 29, for the teaching of memory state and instruction address, see first state and second state in lines 13-20 of column 2, lines 63 of column 8 to line 26 of column 9.

For the reasons set forth in the section 112 rejections above , no statement can be made as to whether the Richter reference meets the functional languages of the claims, although the reference meets the structural limitations. If Applicants disagree with the Examiner's intrepretation of the Richter reference, Applicants are requested to explain word-by-word why the

rejected claims are patentable distinct over the reference (In re Nielson, 816 F.2d 1567, 2USPQ2d 1525 (Fed. Cir. 1987)). Merely pointing out what the calims required is not sufficient to overcome the rejection specifically with the defects set forth in the section 112, rejections.

The Blomgren et al. reference (5,781,750) is cited for the teaching of another dual-instruction-set architecture computer.

DAVID Y. ENG
PRIMARY EXAMINER